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Gated Latch Utilization For Clock Tree Network

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Abstract: **The Major contributor to power dissipation using signal switching of high frequency and strong pipeline designs. Total power consumption using clock tree accounts and 20-40% of power is consumed in synchronous circuits. Therefore, by decreasing the clock-tree power, the chip power reduces. In this proposed system a circuit is implemented which is a frequency synthesizer for generating the clock tree. Then the gated latch technique is applied to this circuit for reducing the power consumption. The resulting output is the generation of the clock tree. The clock power can be controlled through gating. Primary goal is to reduce the power in the clock tree. Thus the clock tree synthesis is performed and gated latch technique is applied to the out coming clock signal from the clock tree. The gated latch is the concept of gating the control signal. The gated signal output plays the role of the enable in the latches. Thus whenever we need we can switch off the clock signal and we can use the clock signal for clock tree synthesis. These are all controlled by the control signal. The power consumed is 0.052.**

Keywords: **Pipeline, signal switching Power dissipation,Clock tree power, Frequency Synthesizer, Gated latch and Control signal**

1. INTRODUCTION

Power consumption is more in many of the circuits/clock distribution. To reduce the usage of power in the clock tree the gated d latch is designed. The gated d latch is designed with a control signal. The control signal is used to switch on or switch off the circuit. In this the clock generator, frequency synthesizer are used. The clock generator is used to generate the clock pulse. From the clock tree many clock pulses are distributed. These clock pulses are synthesized by the frequency synthesizer. The frequency synthesizer performs arithmetic operations such as addition, subtraction, multiplication, division and logical operations such as AND, OR, NAND, NOR, EX-OR, EX-NOR, NOT, etc., the output of the frequency is given to the gated latch to produce the clock tree with a power consumption reduction.

Thus the latches are designed in which it produces the corresponding output when the enable signal is high.

This is the concept of level triggering and it processes on the enable signal which is based on high and low. The gated latch is the concept of gating the control signal. The gated signal output plays the role of the enable in the latches.

Figure1.1 shows that the enable signal has two inputs one is A, and another one is control signal. The value of A is always 1 that is set to be default. Whenever the control signal is 1 the enable signal is 1 and the circuit is ON. If control signal is 0 the enable signal is 0 and the circuit is OFF. Thus whenever we need we can switch off the clock signal and we can use the clock signal for clock tree synthesis. These are all controlled by the control signal. These gated latch controls the clock tree synthesis's unnecessary power consumption.

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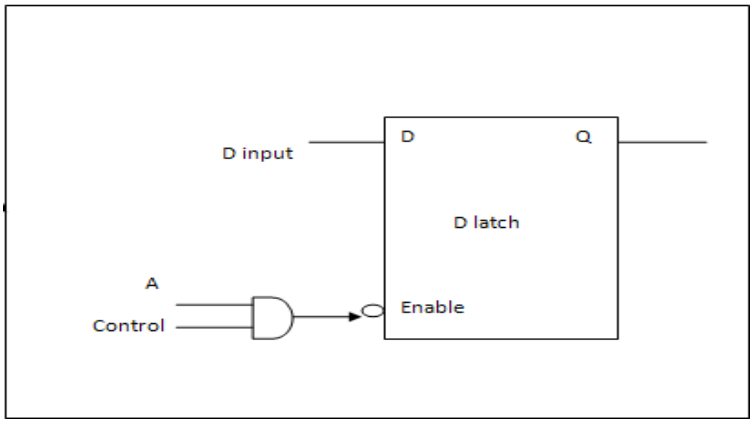

Fig.1 Symbol for gated D latch

2. SYSTEM METHODOLOGY

In this the block diagram for the proposed method is described. The block diagram of the proposed system is shown in Fig. 2 which consists of clock tree generation , frequency synthesizer, Gated D latch respectively.

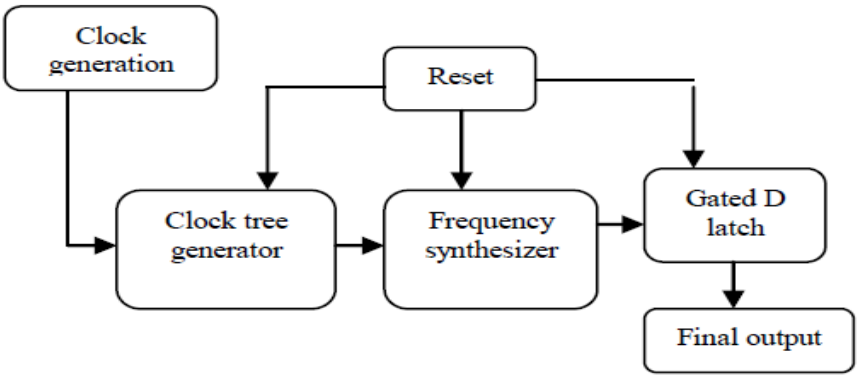

Fig.2 Block Diagram of Proposed System

A. Block Diagram Description:

From the clock generator, the input clock pulse gets generated. In the frequency synthesizer block, we are generating different clock pulses of variable frequencies. Using this, the clock tree generation is performed using a clock tree generator. The distributed clock pulses are given to the gated latch to produce the clock tree with the power consumption reduction. The reset is the condition given for the logical part for initializing.

B. Gated D Latch:

Figure 2 show that a gated D-latch with one-input synchronous SR latch. It is also known as transparent latch, data latch, or simply gated latch.

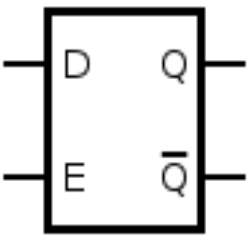

Fig.3 Symbol for Gated D latch

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The truth table shows that when the enable or clock input is 0, the D input has no effect on the output. When Enable/ Control is high, the output equals D.

TABLE.1 TRUTH TABLE FOR GATED D LATCH

E/C	D	Q	Q	Comment
0	X	Q_{prev}	Q_{ns}	NC
1	0	0	1	Reset
1	1	1	0	Set

C. Clock signal:

It is generated by clock generator. A clock signal is a signal which depend upon the 50% of duty cycle and it has two state such as low and high state. It applied for synchronization circuits that may become active at either rising edge or falling edge and in the case of double data rate.

D. Clock Tree:

Clock tree is a tree network which consist sub-tree sections. The power is distributed in the tree and consuming power using clock tree

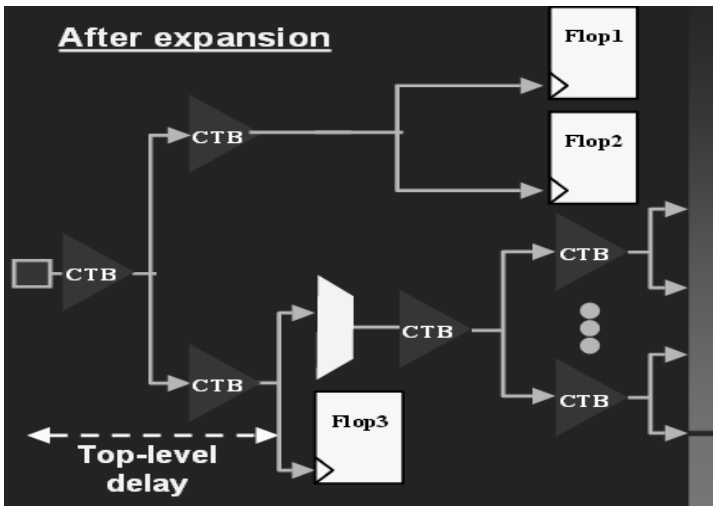

Fig. 4, Flow diagram of model clock tree

E. Clock signal:

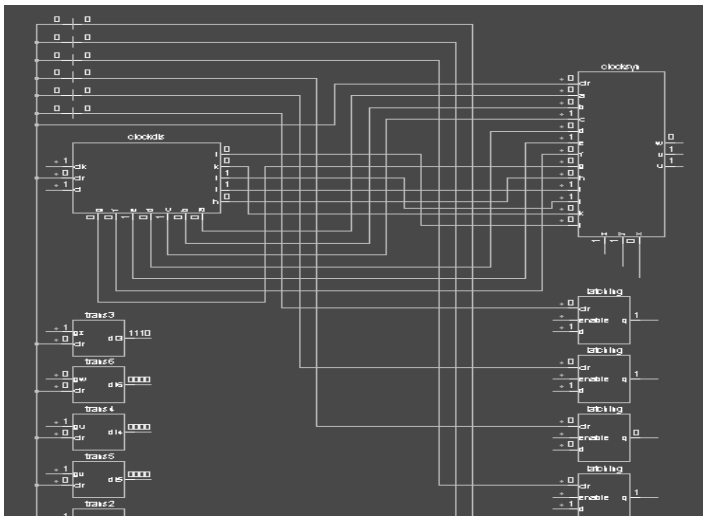

Fig.5 Data flow of proposed system

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This data flow diagram includes clock generation, clock data, data transmission and Gated latch transmission is performed. These are all connected by wires. The data flow has control signals. The control signal is used to control the operation by switching on and off the circuit.

F. Frequency Synthesizer:

It is used to synthesize frequency of electronics component such as CB radios, GPS system, satellite receivers etc. It used to generate different signals not like single signal used in adder, multiplier, etc.

3. COMPUTER SIMULAION RESULTS

The proposed system has been applied for a clock tree. The superiority of the scheme is demonstrated with the help of some example of inputs. In this project, we can use MATLAB ISE. Power report of this project is produced.

Gated latch stage: In this the clock tree is generated using the frequency synthesizer logic. The different set of frequencies is given to the latches to generate the clock tree. The clock distribution network distributes the clock signals from a common point to all the elements that need it.

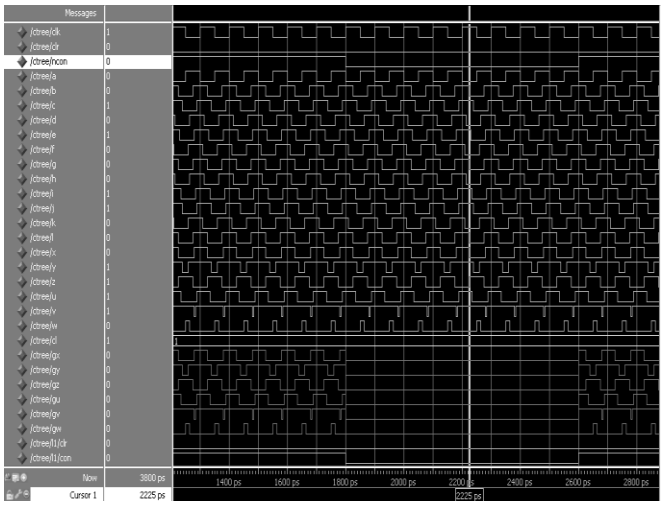

Fig.6 Gated Latch Output

Transmission stage*:* In this frequency synthesizer which produces the set of frequencies as the output. Also the gated latch logic is designed for power consumption reduction. The clock pulses generated are given through the gated latch to produce the clock tree. The gated latch is a latch that has an input that must be active in order for the basic inputs to take effect. This input is sometimes called ENABLE because it enables the operation of the basic inputs. All the sub modules are integrated together and analyzed using modelsim simulator.

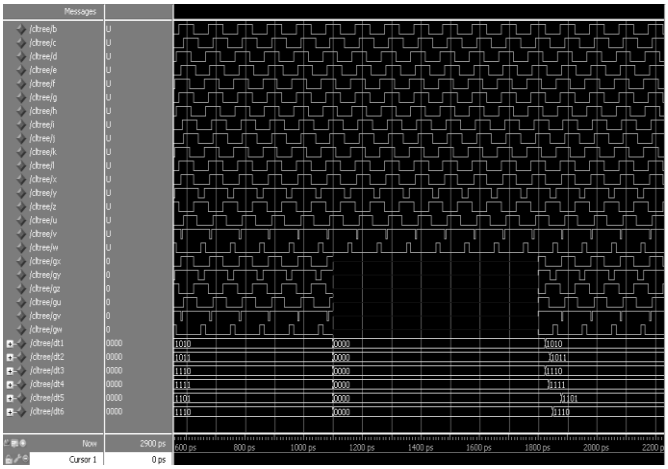

Fig.7,Transmission stage output

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Power report: The power report is shown below. The power is consumed up to 0.052and the report chart is shown.

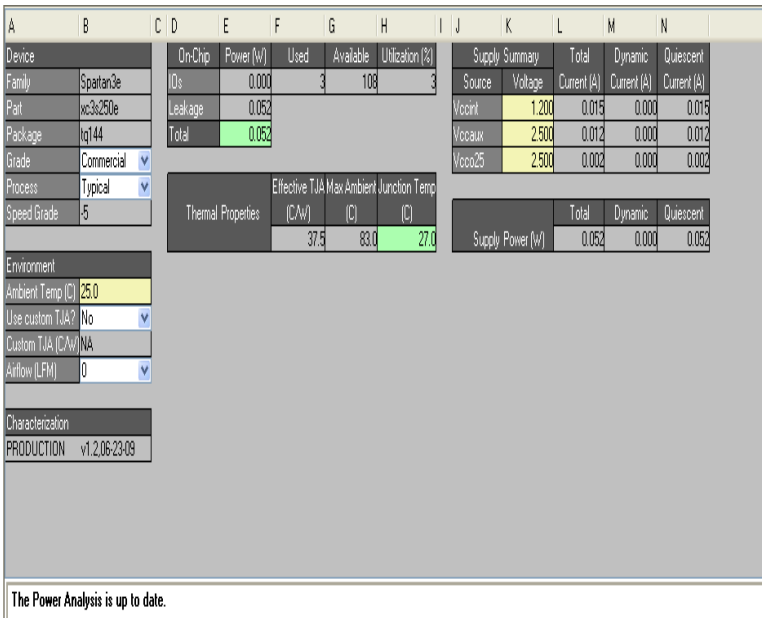

Fig.8 Power Report

4. CONCLUSION

This proposed system has been successfully implemented and evaluated in a clock tree. Here a clock tree module is designed and the frequency synthesizer is performed here to produce different type of clock tree. All the synthesized signal are pass through gated latch to consume power. The power is consumed upto 0.052.

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